CLAIMS

What is claimed is:

1. A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface;

forming a first pattern of conductors and a second pattern of conductors spaced from said first pattern and electrically coupled thereto on said first surface of said first dielectric layer;

forming a common conductive line on said first surface of said first dielectric layer electrically connected to each of said conductors of said second pattern of conductors; and

thereafter terminating said electrical connections between each of said conductors of said second pattern of conductors and said common conductive line using a laser.

2. The method of claim 1 further including positioning a second dielectric layer substantially over said first and second patterns of conductors prior to said terminating of said electrical connections.

3. The method of claim 2 wherein said second dielectric layer is provided in substantially liquid form and flowed onto said first dielectric layer.

4. The method of claim 3 wherein said second dielectric layer comprises a soldermask.

5. The method of claim 2 further including using said laser to simultaneously provide openings in said second dielectric layer above respective ones of said electrical connections during said terminating of said connections.

6. The method of claim 5 wherein said laser also partially removes some of said first dielectric layer immediately below said electrical connections during said terminating of said connections.

7. The method of claim 1 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.

8. The method of claim 1 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.

9. The method of claim 8 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.

10. The method of claim 8 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.

11. A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface;

forming a first pattern of conductors and a second pattern of conductors spaced from said first pattern and electrically coupled thereto on said first surface of said first dielectric layer;

forming a common conductive line on said first surface of said first dielectric layer electrically connected to each of said conductors of said second pattern of conductors by a second conductive line;

positioning a second dielectric layer substantially over said first and second patterns of conductors and common conductive line;

providing openings in said second dielectric layer using a laser to expose at least portions of said conductive lines which electrically couple said second pattern of conductors to said common conductive lines; and

thereafter severing said portions of said conductive lines which electrically couple said second pattern of conductor to said common conductive line.

12. The method of claim 11 wherein said severing of said portions of said conductive lines is accomplished by etching.

13. The method of claim 11 wherein said second dielectric layer is provided in substantially solid form and laminated onto said first dielectric layer.

14. The method of claim 13 wherein said second dielectric layer comprises a soldermask.

15. The method of claim 11 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.

16. The method of claim 11 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.

17. The method of claim 16 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.

18. The method of claim 16 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.

19. A circuitized substrate comprising;

a first dielectric layer having a first surface;

first and second patterns of conductors spacedly positioned on said first surface;

a plurality of connecting lines each connecting one of said conductors in said first pattern of conductors to a respective one of said conductors in said second pattern of conductors;

a common first conductive line on said first surface of said first dielectric layer and a plurality of laser-severed second conductive lines which previously connected said common conductive line to said second pattern of conductors; and

a second dielectric layer positioned on said first surface of said first dielectric layer.

20. The circuitized substrate of claim 19 further including a semiconductor chip positioned on said first dielectric layer and electrically coupled to said first pattern of conductors.

21. The circuitized substrate of claim 19 wherein said first dielectric layer is comprised of fiberglass-reinforced epoxy resin material.

22. The circuitized substrate of claim 19 wherein said first and second patterns of conductors, said common first conductive line and said laser-severed second conductive lines are each comprised of copper.

23. The circuitized substrate of claim 19 wherein said second dielectric layer is comprised of soldermask material.

24. An information handling system comprising an electronic package including a circuitized substrate having a first dielectric layer having a first surface, first and second patterns of conductors spacedly positioned on said first surface, a plurality of connecting lines each connecting one of said conductors in said first pattern of conductors to a respective one of said conductors in said second pattern of conductors, a common first conductive line on said first surface of said first dielectric layer and a plurality of laser-severed second conductive lines which previously connected said common conductive line to said second pattern of conductors, and a second dielectric layer positioned on said first surface of said first dielectric layer.

25. The information handling system of claim 24 further including a printed circuit board, said electronic package being positioned on and electrically coupled to said printed circuit board.

26. A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface and a second opposing surface;

forming a first pattern of conductors and a second pattern of conductors spaced from said first pattern and electrically coupled thereto on said first surface of said first dielectric layer;

forming a common conductive line on said second opposing surface of said first dielectric layer and electrically connected to each of said conductors of said second pattern of conductors; and

thereafter terminating said electrical connections between each of said conductors of said second pattern of conductors and said common conductive line using a laser.

27. The method of claim 26 further including positioning a second dielectric layer substantially over said first and second patterns of conductors and a third dielectric layer over said common conductive line prior to said terminating of said electrical connections.

28. The method of claim 27 wherein said second and third dielectric layers are provided in substantially liquid form and flowed onto said first dielectric layer.

29. The method of claim 28 wherein said second and third dielectric layers each comprise a soldermask.

30. The method of claim 27 further including using said laser to simultaneously provide openings above respective ones of said electrical connections during said terminating of said connections.

31. The method of claim 30 wherein said laser also partially removes some of said first dielectric layer immediately below said electrical connections during said terminating of said connections.

32. The method of claim 26 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.

33. The method of claim 26 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.

34. The method of claim 33 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.

35. The method of claim 33 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.

36. A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface and a second opposing surface;

forming a first pattern of conductors and a second pattern of conductors spaced from said first pattern and electrically coupled thereto on said first surface of said first dielectric layer;

forming a common conductive line on said second opposing surface of said first dielectric layer and electrically connected to each of said conductors of said second pattern of conductors by a second conductive line;

positioning a second dielectric layer substantially over said first and second patterns of conductors and a third dielectric layer over said common conductive line;

providing openings using a laser to expose at least portions of said conductive lines which electrically couple said second pattern of conductors to said common conductive lines; and

thereafter severing said portions of said conductive lines which electrically couple said second pattern of conductors to said common conductive line.

37. The method of claim 36 wherein said severing of said portions of said conductive lines is accomplished by etching.

38. The method of claim 37 wherein said second dielectric layer is provided in substantially liquid form and flowed onto said first dielectric layer.

39. The method of claim 38 wherein said second and third dielectric layers each comprise a soldermask.

40. The method of claim 36 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.

41. The method of claim 36 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.

42. The method of claim 41 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.

43. The method of claim 41 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.

44. A circuitized substrate comprising;

a first dielectric layer having a first surface and a second, opposing surface;

first and second patterns of conductors spacedly positioned on said first surface;

a plurality of connecting lines each connecting one of said conductors in said first pattern of conductors to a respective one of said conductors in said second pattern of conductors;

a common first conductive line on said second opposing surface of said first dielectric layer and a plurality of laser-severed second conductive lines which previously connected said common conductive line to said second pattern of conductors; and

second and third dielectric layers positioned on said first and said second opposing surfaces of said first dielectric layer, respectively.

45. The circuitized substrate of claim 44 further including a semiconductor chip positioned on said first dielectric layer and electrically coupled to said first pattern of conductors.

46. The circuitized substrate of claim 44 wherein said first dielectric layer is comprised of fiberglass-reinforced epoxy resin material.

47. The circuitized substrate of claim 44 wherein said first and second patterns of conductors, said common first conductive line and said laser-severed second conductive lines are each comprised of copper.

48. The circuitized substrate of claim 44 wherein said second and third dielectric layers are each comprised of soldermask material.

49. An information handling system comprising an electronic package including a circuitized substrate having a first dielectric layer having a first surface and a second opposing surface, first and second patterns of conductors spacedly positioned on said first surface, a plurality of connecting lines each connecting one of said conductors in said first pattern of conductors to a respective one of said conductors in said second pattern of conductors, a common first conductive line on said second opposing surface of said first dielectric layer and a plurality of laser-severed second conductive lines which previously connected said common conductive line to said second pattern of conductors, and second and third dielectric layers positioned on said first and second opposing surfaces of said first dielectric layer, respectively.

50. The information handling system of claim 49 further including a printed circuit board, said electronic package being positioned on and electrically coupled to said printed circuit board.

51. A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface and a second opposing surface;

forming a first pattern of conductors on said first surface and a second pattern of conductors on said second surface and electrically coupled to said first pattern of conductors on said first dielectric layer;

forming a common conductive line on said second opposing surface of said first dielectric layer electrically connected to each of said conductors of said second pattern of conductors; and

thereafter terminating said electrical connections between each of said conductors of said second pattern of conductors and said common conductive line using a laser.

52. The method of claim 51 further including positioning a second dielectric layer substantially over said first pattern of conductors and a third dielectric layer over said second pattern of conductors and said common conductive line prior to said terminating of said electrical connections.

53. The method of claim 52 wherein said second and third dielectric layers are provided in substantially liquid form and flowed onto said first dielectric layer.

54. The method of claim 53 wherein said second and third dielectric layers each comprise a soldermask.

55. The method of claim 52 further including using said laser to simultaneously provide openings above respective ones of said electrical connections during said terminating of said connections.

56. The method of claim 55 wherein said laser also partially removes some of said first dielectric layer immediately below said electrical connections during said terminating of said connections.

57. The method of claim 51 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.

58. The method of claim 51 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.

59. The method of claim 58 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.

60. The method of claim 58 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.

61. A method of making a circuitized substrate, said method comprising:

providing a first dielectric layer having a first surface and a second opposing surface;

forming a first pattern of conductors on said first surface and a second pattern of conductors on said second opposing surface and electrically coupled to said first pattern of conductors on said first dielectric layer;

forming a common conductive line on said second opposing surface of said first dielectric layer electrically connected to each of said conductors of said second pattern of conductors by a second conductive line;

positioning a second dielectric layer substantially over said first pattern of conductors and a third dielectric layer over said second pattern of conductors and common conductive line;

providing openings in said third dielectric layer using a laser to expose at least portions of said conductive lines which electrically couple said second pattern of conductors to said common conductive lines; and

thereafter severing said portions of said conductive lines which electrically couple said second pattern of conductor to said common conductive line.

62. The method of claim 61 wherein said severing of said portions of said conductive lines is accomplished by etching.

63. The method of claim 61 wherein said second dielectric layer is provided in substantially liquid form and flowed onto said first dielectric layer.

64. The method of claim 63 wherein said second and third dielectric layers each comprise a soldermask.

65. The method of claim 61 wherein said first and second pattern of conductors and said common conductive line are formed using electrolytic plating.

66. The method of claim 61 further including positioning a semiconductor chip on said first dielectric layer and electrically coupling said semiconductor chip to said first pattern of conductors.

67. The method of claim 66 wherein said electrically coupling of said semiconductor chip to said first pattern of conductors is accomplished using a wirebonding operation.

68. The method of claim 66 wherein said semiconductor chip is electrically coupled to said first pattern of conductors using a plurality of solder balls.

69. A circuitized substrate comprising;

a first dielectric layer having a first surface and a second opposing surface;

a first pattern of conductors positioned on said first surface;

a second pattern of conductors position on said second surface;

a plurality of connecting lines each connecting one of said conductors in said first pattern of conductors to a respective one of said conductors in said second pattern of conductors;

a common first conductive line on said second surface of said first dielectric layer and a plurality of laser-severed second conductive lines which previously connected said common conductive line to said second pattern of conductors; and

second and third dielectric layers positioned on said first and second opposing surfaces of said first dielectric layer, respectively.

70. The circuitized substrate of claim 69 further including a semiconductor chip positioned on said first dielectric layer and electrically coupled to said first pattern of conductors.

71. The circuitized substrate of claim 69 wherein said first dielectric layer is comprised of fiberglass-reinforced epoxy resin material.

72. The circuitized substrate of claim 69 wherein said first and second patterns of conductors, said common first conductive line and said laser-severed second conductive lines are each comprised of copper.

73. The circuitized substrate of claim 69 wherein said second and third dielectric layers are each comprised of soldermask material.

74. An information handling system comprising an electronic package including a circuitized substrate having a first dielectric layer having a first surface and a second opposing surface, a first pattern of conductors positioned on said first surface, a second pattern of conductors positioned on said second opposing surface, a plurality of connecting lines each connecting one of said conductors in said first pattern of conductors to a respective one of said conductors in said second pattern of conductors, a common first conductive line on said second opposing surface of said first dielectric layer and a plurality of laser-severed second conductive lines which previously connected said common conductive line to said second pattern of conductors, and second and third dielectric layers positioned on said first and second opposing surfaces of said first dielectric layer, respectively.

75. The information handling system of claim 74 further including a printed circuit board, said electronic package being positioned on and electrically coupled to said printed circuit board.